REMARKS

Claims 2-5, 9-12, 16-20 and 22-24 are pending. No claims have been amended or canceled by this amendment.

Claim Rejections 35 USC §103

Claims 2-5, 9-12, 16-20 and 22-24 stand rejected under 35 USC §103(a) as being unpatentable over Steinmetz (U.S. Pat. no. 5,600,579) in view of Pickup (U.S. Pat. no. 5,774,380). Applicant respectfully traverses this rejection.

Steinmetz teaches compiling the master model computer program to produce the master model, wherein the step of compiling the master model computer program includes accessing the shared library functions to retrieve object code corresponding to at least one of the plurality of predefined verification system functions invoked by the master model computer program.

It teaches accessing library functions to retrieve object code, it does not teach compiling the master model itself into object code. In fact, Steinmetz teaches away from compiling the master model into object code. See col. 1, lines 43-57, where the specification, in discussing the prior art, notes that the master model emulates a CPU (implemented either in HDL or as a gate level model). Testing a modeled circuit under this circumstance requires that the assembly language instructions of the master model be compiled into binary object code, and the binary code loaded into memory. However, the specification goes on to describe the drawbacks of such an approach including: the inability to directly manipulate Verilog wires, registers, and time, and the need to use many instructions to perform a single task. See col. 1, line 59 through col. 2, line 4. In view of the above, it is clear that Steinmetz teaches away from converting HDL coded electronic circuit model portions to binary object code.

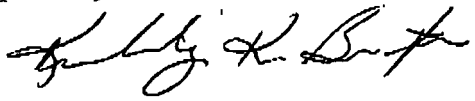
Further, the Pickup reference refers to the ability to capture or assign a "state" of operation to a circuit portion during simulation so that the state may then be used in another simulation, see col. 1, lines 10-13. The saving of "states" of the circuit portions or sequential devices is performed through use of a storage file, see col. 2, lines 35-38. This is not a compiling function as claimed by the present claims and there is no discussion of compiling anything into binary object code. The Pickup reference describes using the Verilog HDL with a Verilog compatible simulator which eliminates any need for compiling of a modeled circuit that has been coded in Verilog HDL. As such, applicant submits that Pickup does not provide the teachings that the office action proposes and that, since Pickup does not relate to compiling, it is inappropriately combined with Steinmetz.

In view of the arguments presented with respect to the independent claims 22-24, the remaining rejections to dependent claims have not been specifically addressed.

In view of the foregoing, it is submitted that this application is in condition for allowance. Favorable consideration and prompt allowance of the application are respectfully requested.

The Examiner is invited to telephone the undersigned if the Examiner believes it would be useful to advance prosecution.

Respectfully submitted,



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